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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/466,934	12/20/99	YAMAGUCHI Y	0057-2567-2Y

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EXAMINER	
STEVENSON, A	
ART UNIT	**PAPER NUMBER**
2812	5

DATE MAILED: 02/12/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/466,934	YAMAGUCHI ET AL.	
	Examiner	Art Unit	
	Andre' Stevenson	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-23 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a)☐ All b)☐ Some * c)☐ None of the CERTIFIED copies of the priority documents have been:

1.☐ received.

2.☐ received in Application No. (Series Code / Serial Number) _____ .

3.☐ received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

Attachment(s)

15)☒ Notice of References Cited (PTO-892)
16)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17)☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
18)☐ Interview Summary (PTO-413) Paper No(s). _____ .
19)☐ Notice of Informal Patent Application (PTO-152)
20)☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1 through 23 are rejected under 35 U.S.C. 102(e) as being unpatentable over Saito (U.S. Pat. No.6100570).

Saito (U.S. Pat. No.6100570), for **Claim #1**, teaches a device having SOI stucture, buried insulation layer, plurality of device formation regions being provided in SOI, at least one isolation region, a body region provided in SOI and at least part of at least one isolation region includes partial isolation region, (*figure #20, reference 201& 202, column 6 lines 53 through 58 & figure #3, reference 36& 39, column 8 lines 34 through 42 & figure #7, reference 71, 73& 77, column 9 lines 1 through 5*).

With respect to **Claim #2**, a device wherein plurality of device formation regions include a plurality of first device formation regions for a first device, a plurality of second device formation regions for a second device, wherein plurality of first device formation regions are isolated (*figure #29a, reference 291 – 296, column 2 lines 23 through 31 & & figure #7, reference 71, 73& 77, figure #4a, reference 41 – 50, column 9 lines 48*

through 59) Saito discloses a device wherein plurality of device formation regions include a plurality of first device formation regions for a first device and a plurality of second device formation regions for a second device, wherein plurality of first device formation regions are isolated.

Furthermore, **Claim #3**, wherein plurality of device regions include a plurality of device formation regions for first and second circuit, regions for first and second circuit are isolated from each other, (*figure #4a, reference 41 – 50, column 9 lines 48 through 59*) Saito teaches a device wherein plurality of device regions include a plurality of device formation regions for first and second circuit, regions for first and second circuit are isolated from each other.

Considering now **Claim #4**, wherein plurality of device regions for a predetermined circuit and for a circuit other than predetermined circuit, device regions are isolated from each other, (*figure #6 reference 61 - 68, column #10 lines 36 through 54*), Saito teaches a device wherein plurality of device regions for a predetermined circuit and for a circuit other than predetermined circuit, device regions are isolated from each other.

With respect to **Claim #5**, a device wherein at least one isolation region includes a plurality of isolation regions, (*figure #29a, reference 291 – 296, column 2 lines 23 through 31)* Saito discloses a device wherein at least one isolation region includes a plurality of isolation regions.

Furthermore, **Claim #6**, wherein plurality of device formation regions which predetermined devices are formed, at least one isolation region provided in SOI layer, a

body region capable of externally fixing electric potential, body region is formed in contact with one of top and bottom surfaces, (*figure #20, reference 201& 202, column 6 lines 53 through 58 & figure #3, reference 36& 39, column 8 lines 34 through 42 & figure #7, reference 71, 73& 77, column 9 lines 1 through 5 & figure #29a, reference 291 – 296, column 2 lines 23 through 31*) Saito teaches a device wherein plurality of device formation regions which predetermined devices are formed, at least one isolation region provided in SOI layer, a body region capable of externally fixing electric potential, body region is formed in contact with one of top and bottom surfaces.

Considering now **Claim #7**, wherein at least part of isolation region including partial isolation region and complete insulation region extending through SOI layer, (*figure #20, reference 201& 202, column 6 lines 53 through 58 & figure #3, reference 36& 39, column 8 lines 34 through 42 & figure #7, reference 71, 73& 77, column 9 lines 1 through 5 & figure #29a, reference 291 – 296, column 2 lines 23 through 31*), Saito teaches a device wherein at least part of isolation region including partial isolation region and complete insulation region extending through SOI layer.

With respect to **Claim #8**, a device wherein partial isolation region has a flat and even top surface, (*figure #29a&b, column 2 lines 23 through 31)* Saito discloses a wherein partial isolation region has a flat and even top surface.

Furthermore, **Claim #9**, wherein semiconductor region has a thickness which is not greater than one-half thickness of SOI layer, (*figure #20, reference 201- 202, column 6 lines 53 through 58*) Saito teaches a device wherein semiconductor region has a thickness which is not greater than one-half thickness of SOI layer.

Considering now **Claim #10**, wherein insulation region of combined isolation region has width not greater that one half the width of combined isolation region, (*figure #5 reference 42, column #11 lines 7 through 19*), Saito teaches a device wherein insulation region of combined isolation region has width not greater that one half the width of combined isolation region.

With respect to **Claim #11**, a device wherein complete isolation region having complete insulation region extending through SOI layer, plurality of device formation regions include input/output NMOS transistor, isolation region formed in vicinity of boundary between input/output NMOS transistor and input/output PMOS transistor, (*figure #2, reference 21 – 28, column 9 lines 18 through 34)* Saito discloses a device wherein complete isolation region having complete insulation region extending through SOI layer, plurality of device formation regions include input/output NMOS transistor, isolation region formed in vicinity of boundary between input/output NMOS transistor and input/output PMOS transistor.

Furthermore, **Claim #12**, wherein plurality of device regions include internal circuit formation region, isolation region in the vicinity of boundary between internal circuit formation region and input/output NMOS and input/output PMOS, (*figure #2, reference 21 – 28, column 9 lines 18 through 34*) Saito teaches a device wherein plurality of device regions include internal circuit formation region, isolation region in the vicinity of boundary between internal circuit formation region and input/output NMOS and input/output PMOS.

Considering now **Claim #13**, wherein plurality of device isolation region having complete insulation region extending through SOI layer, plurality of device formation regions include NMOS transistor, isolation region formation location situated within PMOS transistor, isolation region surrounds NMOS transistor formation region and PMOs transistor formation region, (*figure #2, reference 21 – 28, column 9 lines 18 through 34*), Saito teaches a device wherein isolation region having complete insulation region extending through SOI layer.

With respect to **Claim #14**, a device that includes transistor formation region of first conductivity type, isolation region surrounding transistor region, peripheral body region of second conductivity type surrounding peripheral partial isolation region, (*figure #25, reference 252, 255, 256 & 260-262, column 1 lines 46 through 54)* Saito discloses a device wherein transistor formation region of first conductivity type, isolation region surrounding transistor region, peripheral body region of second conductivity type surrounding peripheral partial isolation region.

Furthermore, **Claim #15**, wherein plurality formation region include MOS transistor formation region, body region includes an adjacent to source body region disposed adjacent to source region of MOS transistor region, electric potential setting region, (*figure #2, reference 21- 28, column 9 lines 18 through 28 & figure #3, reference 31- 35, column 8 lines 24 through 38*) Saito teaches a device wherein plurality formation region include MOS transistor formation region, body region includes an adjacent to source body region disposed adjacent to source region of MOS transistor region, electric potential setting region.

Considering now **Claim #16**, wherein semiconductor region includes first and second partial semiconductor regions, first partial semiconductor region is higher that second partial semiconductor region, (*figure #1 reference 13, column #7 lines 66,67 column #8 lines 1 through 9*), Saito teaches a device wherein semiconductor region includes first and second partial semiconductor regions, first partial semiconductor region is higher that second partial semiconductor region.

With respect to **Claim #17**, a device formation regions include MOS tranasistor formation region of first conductivity type, peak impurity concentration is deeper from surface of SOI layer that peak of impurity concentration drain/source, (*figure #2, reference 21 – 28, column 9 lines 18 through 28)* Saito discloses a device formation regions include MOS tranasistor formation region of first conductivity type, peak impurity concentration is deeper from surface of SOI layer that peak of impurity concentration drain/source.

Furthermore, **Claim #18**, wherein plurality device formation regions include MOS transistor formation region, impurity concentration of channel region is deeper form surface of SOI layer that peak of impurity concentration of semiconductor region of isolation region, (*figure #3, reference 31- 34, column 8 lines 24 through 34*) Saito teaches a device wherein plurality of device formation regions include MOS transistor formation region, impurity concentration of channel region is deeper form surface of SOI layer that peak of impurity concentration of semiconductor region of isolation region.

Considering now **Claim #19**, wherein surface corner part and bottom corner part having radius of curvature greater than that of surface corner part, (*figure #8, column*

#11 lines 8 through 11 & figure #7, column #9 lines 1 through 5), Saito teaches a device wherein surface corner part and bottom corner part having radius of curvature greater than that of surface corner part.

With respect to **Claim #20**, a device wherein isolation region has bottom corner part and stepped part defined between complete insulation region and partial insulation region, (*figure #8, column #11 lines 8 through 11 & figure #7, column #9 lines 1 through 5)* Saito discloses a device wherein isolation region has bottom corner part and stepped part defined between complete insulation region and partial insulation region.

Furthermore, **Claim #21**, wherein complete isolation region having insulation region extending through SOI layer, inductance element formed, complete isolation region is formed under inductance formation region, (*figure #8, reference 84, column 11 lines 19 through 21*) Saito teaches a device wherein complete isolation region having insulation region extending through SOI layer, inductance element formed, complete isolation region is formed under inductance formation region.

Considering now **Claim #22**, wherein plurality of device regions include MOS transistor formation region, gate-connected body region electrically connected, partial isolation region surrounds MOS transistor formation region, (*figure #1, reference 15 – 18, column 6 lines 44 through 52*), Saito teaches a device having MOS transistor formation region, gate-connected body region electrically connected, partial isolation region surrounds MOS transistor formation region.

With respect to **Claim #23**, a device wherein predetermined device formed in SOI layer, (*figure #2, reference 21 – 28, column 9 lines 18 through 34, figure #8, column*

11 lines 8 through 11 & figure #7, column 9 lines 1 through 15) Saito discloses a device wherein predetermined device formed in SOI layer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andre' Stevenson whose telephone number is (703) 308 6227. The examiner can normally be reached on Monday through Friday from 7:30 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling, can be reached on (703) 308 3325. The fax phone number for the organization where this application or proceeding is assigned is (703) 308 7724.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308 0956.

John F. Niebling
Supervisory Patent Examiner
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Andre' Stevenson

Art Unit 2812

12/22/00